

## REMARKS

Applicant thanks the Examiner for indicating allowable subject matter, in light of which applicant has cancelled without prejudice claims 5-9 that were previously withdrawn from consideration. Applicant has amended claim 4 to overcome the claim objection. Claims 1 and 2 have been amended to improve English usage without changing claim scope. Applicant has added new claim 10, which finds support, for example, at page 4, lines 23-27, of the specification and FIG. 2A of the application.

Claims 1 and 2 have been rejected under 35 USC 102(b) as anticipated by U.S. Patent No. 5,990,629 (Yamada). Applicant respectfully traverses this rejection.

To anticipate a claim, the reference must teach every element of the claim. MPEP 2131. The standard for the anticipation analysis is that “[e]very element of the claimed invention must be literally present, arranged as in the claim. ... The identical invention must be shown in as complete detail as is contained in the patent claim.” *Richardson v. Suzuki Motor Co., Ltd.*, 868 F.2d 1226, 1236 (Fed. Cir. 1983).

Claim 1 states that the pixel selecting transistor comprises an active layer made of polysilicon, and the driving transistor comprises an active layer made of amorphous silicon. The Examiner contends that Yamada’s semiconductor layer 13d of selection transistor 13 corresponds to the claimed active layer of the pixel selecting transistor and Yamada’s semiconductor layer 12d of drive transistor 12 to the claimed active layer of the driving transistor. See page 3 of the Action. Under *Richardson*, for Yamada to anticipate the claimed invention, Yamada must disclose that the semiconductor layer 13d is made of polysilicon and the semiconductor layer 12d is made of amorphous silicon.

The Examiner contends that Yamada disclose this claim limitation at column 7, lines 25-55. Applicant respectfully disagrees. All Yamada says about its semiconductor layers 12d and 13d is:

A semiconductor layer 13d made of amorphous silicon or polysilicon is formed on the gate insulating film 14b in the upper side of the gate electrode 13a.  
... A semiconductor layer 12d made of amorphous silicon or polysilicon is formed on the gate insulating film 14b above the gate electrode 12a.

No part of Yamada requires the semiconductor layer 13d of the selection transistor 13 to be made of polysilicon and the semiconductor layer 12d of the drive transistor 12 to be made of amorphous silicon, as claimed. Rather, based on the Yamada's statement that the semiconductor layers 12d and 13d are made of "amorphous silicon or polysilicon," persons of ordinary skill in the art would have understood that each of Yamada's semiconductor layers 12d and 13d is made of the same type of silicon, whether it is polysilicon or amorphous silicon. In fact, Yamada does not disclose any process step to produce two different types of active layers, i.e., polysilicon and amorphous silicon, such as the one explained at page 5, line 21 - page 6, line 7, of the specification.

Claim 2 presents the functional features of the structure recited in claim 1 so as to provide claim scope corresponding to both the polysilicon/amorphous configuration and the polysilicon/polysilicon configuration. The rejection of claims 1 and 2 under 35 USC 102(b) on Yamada should be withdrawn because under *Richardson* Yamada fails to disclose the claim limitations relating to the selecting transistor and the drive transistor.

In light of the above, a Notice of Allowance is solicited.

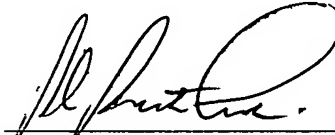
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Respectfully submitted,

Dated: December 18, 2006

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